CLAIMS

We claim:

1. Logic circuitry in a computer, the logic circuitry comprising means for distinguishing between multiple reset commands issued by a primary computer and by said computer, and means for inhibiting all but one of said reset commands from resetting said computer at any one time.

2. The logic circuitry of claim 1, further comprising:

a power on/off signal line originating from said primary computer;

one or more decode modules which interpret commands received from said primary computer;

one or more programmable registers which assume a prescribed state in response to said interpreted commands and said power on/off signal line;

one or more AND gates which output a signal indicative of the status of said decode module and said programmable register;

one or more OR gates which applies a reset signal to the components of the computer, in response to the status of said AND gate, said programmable and said power on/off line.

3. Logic circuitry of claim 2, further comprising an explicit reset line controlled by said primary computer and input to said OR gate.

4. A modular computer network system comprising:

a primary computer; and

one or more modular computer units, equipped with logic circuitry enabling said primary computer to issue reset commands to a subset of the equipped modular computer units.

5. The modular computer network of claim 4, further comprising:

a power on/off signal line originating from said primary computer;

one or more decode modules which interpret commands received from said primary computer;

one or more programmable registers which assume a prescribed state in response to said interpreted commands and said power on/off signal line;

one or more AND gates which output a signal indicative of the status of said decode module and said programmable register;

one or more OR gates which applies a reset signal to the components of the target computer, in response to the status of said AND gate, said programmable and said power on/off line.

6. The modular computer network of claim 6, further comprising an explicit reset line controlled by said primary computer and input to said OR gate.

7. The modular computer network of claim 6, wherein the modular computer units are connected through a common shared memory.

8. The modular computer network of claim 6, wherein the modular computer units are connected by a parallel bus.

9. The modular computer network of claim 6, wherein the modular computer units are synchronized by the primary computer, by the issuance of explicit reset commands.

10. The modular computer network of claim 6, wherein the modular computer units are synchronized by the issuance of a reset command.

11. The modular computer network of claim 6, wherein the modular computer units comprise more than one processing device per module.

12. The modular computer network of claim 6, wherein the modular computer units are arranged in a hierarchy, with one modular computer unit controlling groups of subordinate computer units.

13. A computer system comprising a host computer and plural client computers, at least one of said client computers including circuitry for monitoring said host computer, and for detecting a fault state, and transmission circuitry for transmitting a reset signal to said host computer from said at least one client computer in response to detecting said fault.

14. The computer system of claim 13 wherein said circuitry for detecting includes circuitry for monitoring a clock signal being utilized by said host computer.

15. The computer system of claim 13 wherein said circuitry for detecting includes circuitry for monitoring a clock signal being utilized by said host computer.

16. The computer system of claim 13 wherein said circuitry for detecting includes circuitry for receiving a signal from a source other than said host, over a network, in order to indicate a fault with the host.

17. The computer system of claim 13 wherein the circuitry for detecting includes circuitry for executing a diagnostic software program.

18. The computer system of claim 13 further comprising circuitry for configuring said client computer as a host computer in response to detecting a fault with the host computer.